

Fig. 1.

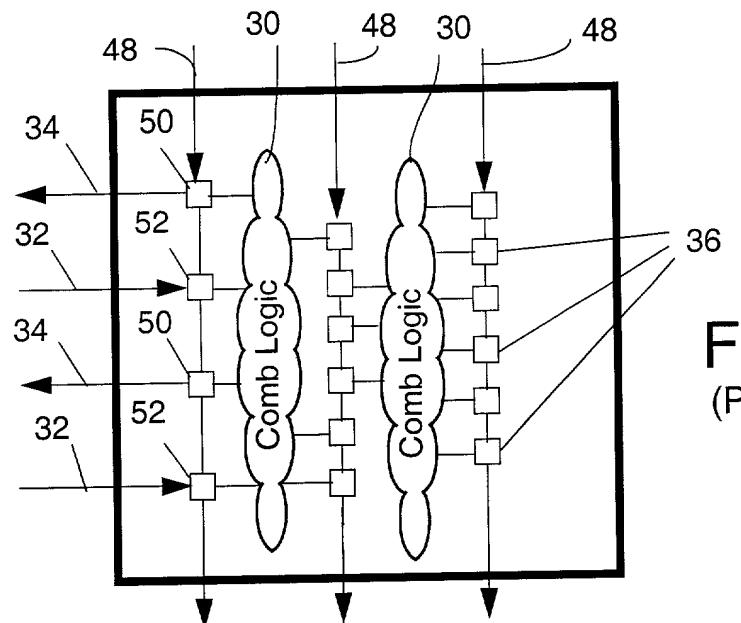


Fig. 2.
(Prior Art)

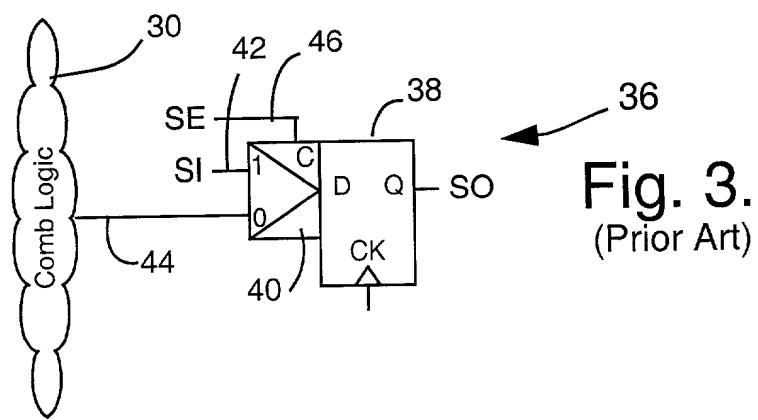


Fig. 3.
(Prior Art)

Fig. 4.

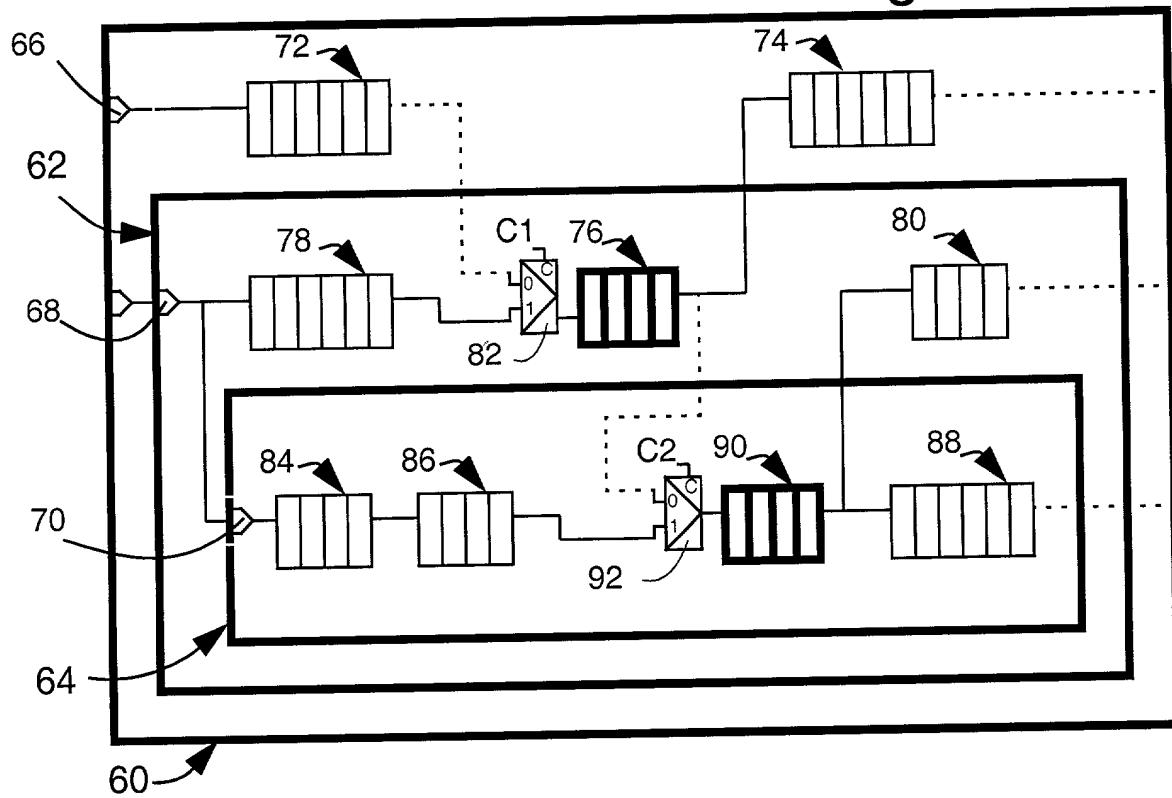


Fig. 5.

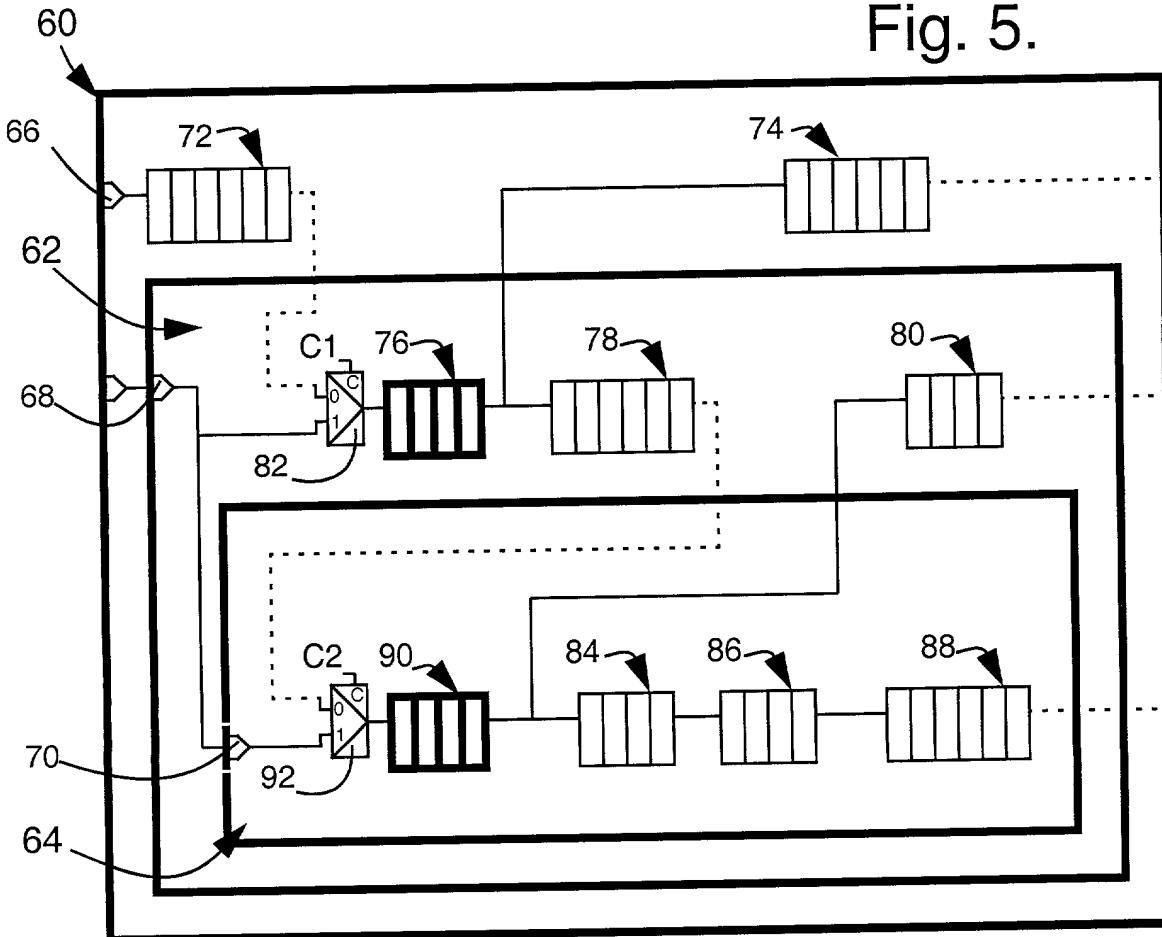


Fig. 6.

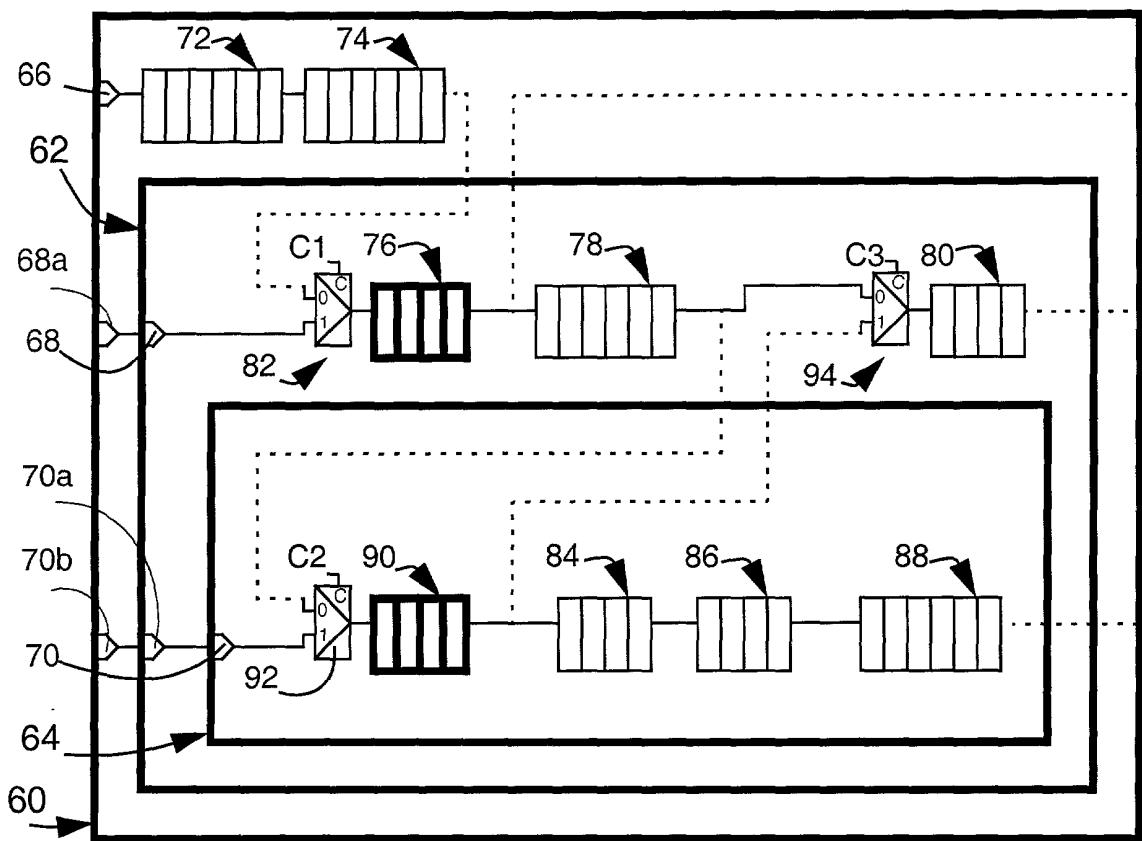


Fig. 7.

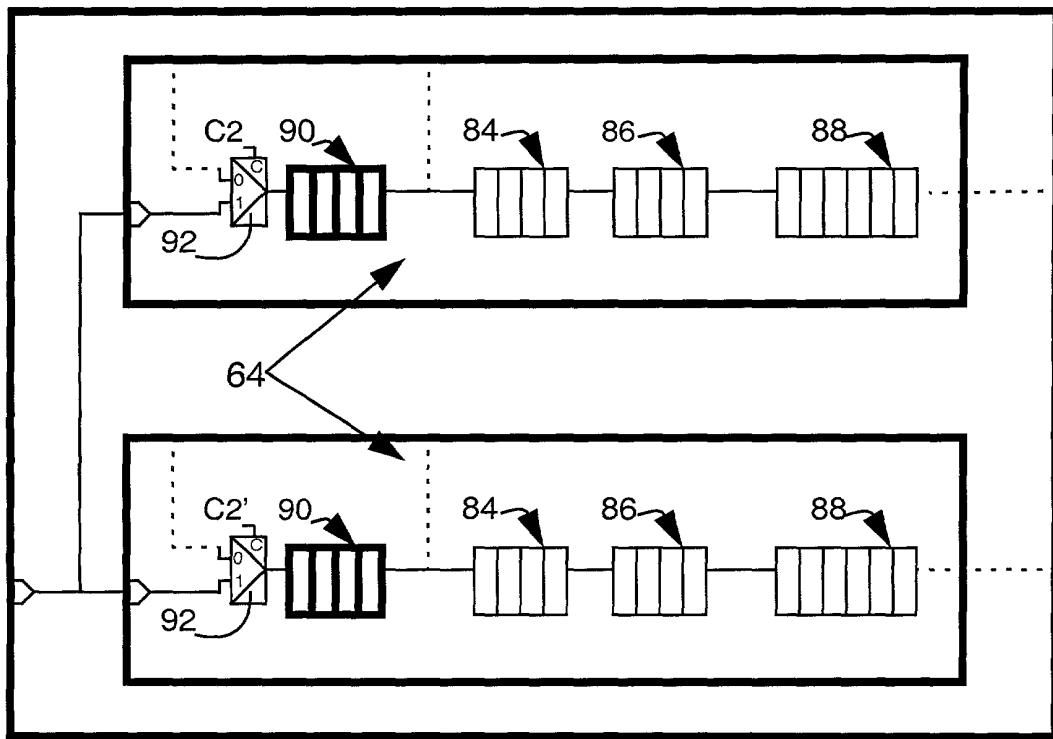


Fig. 8.

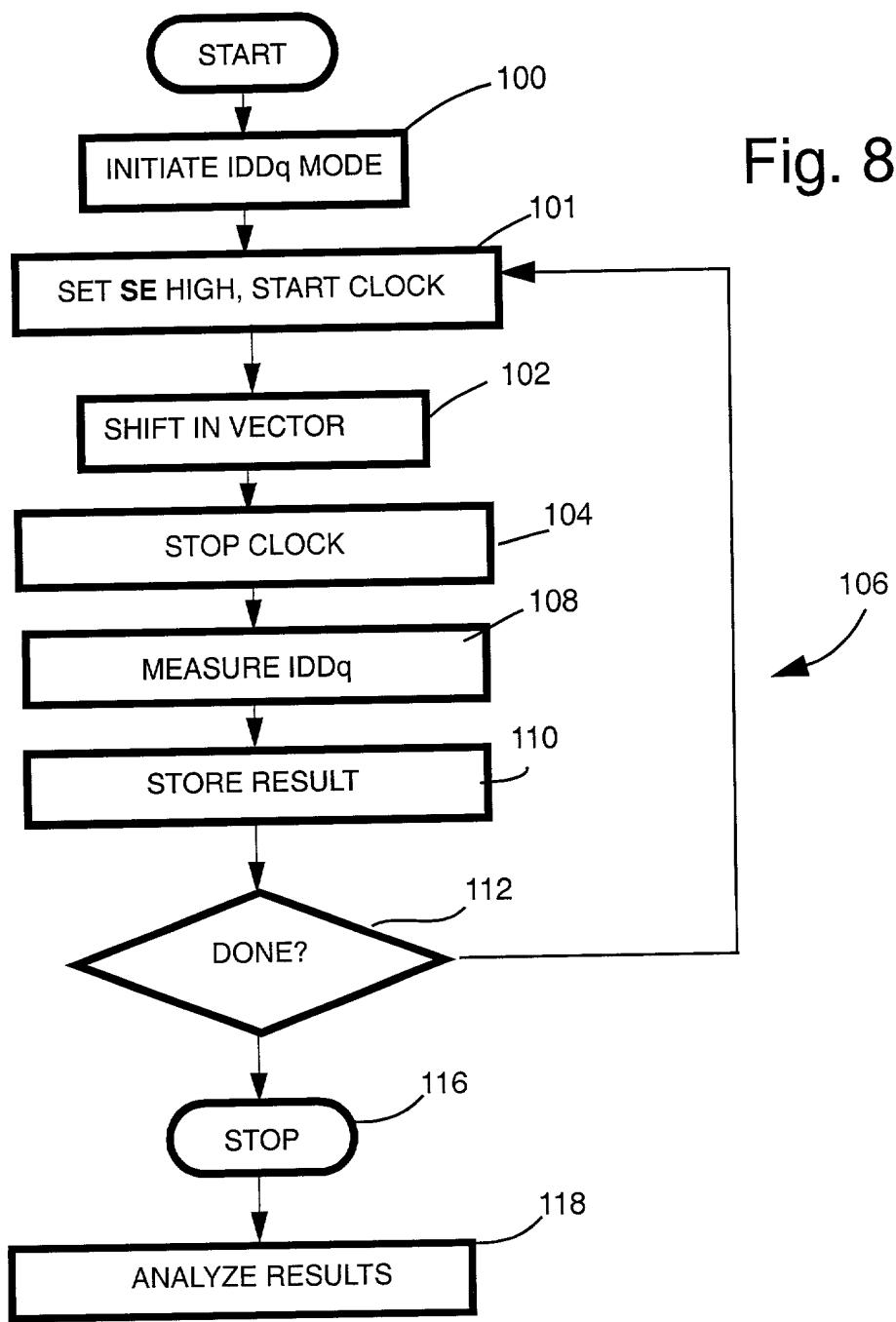


Fig. 9.

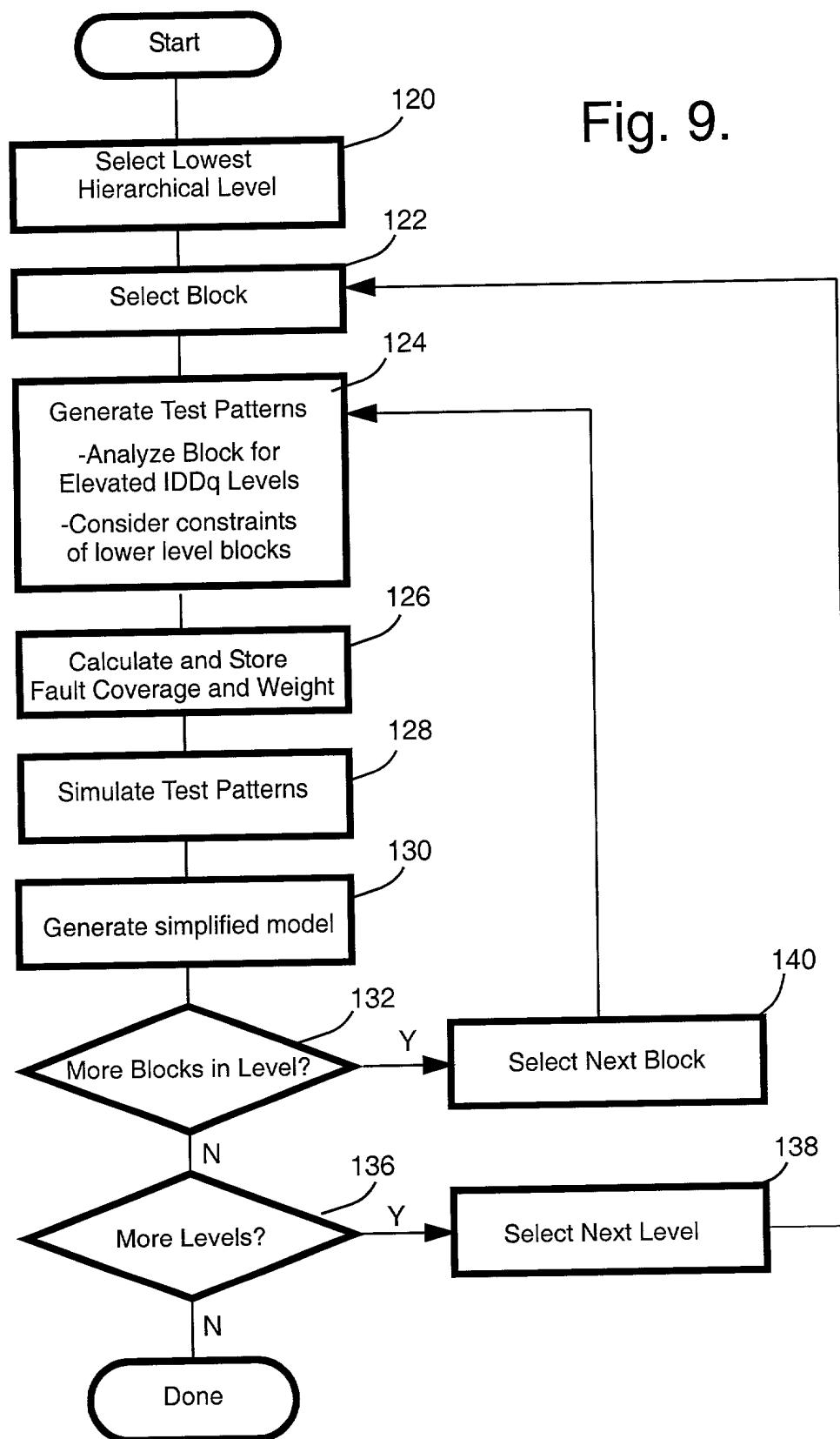
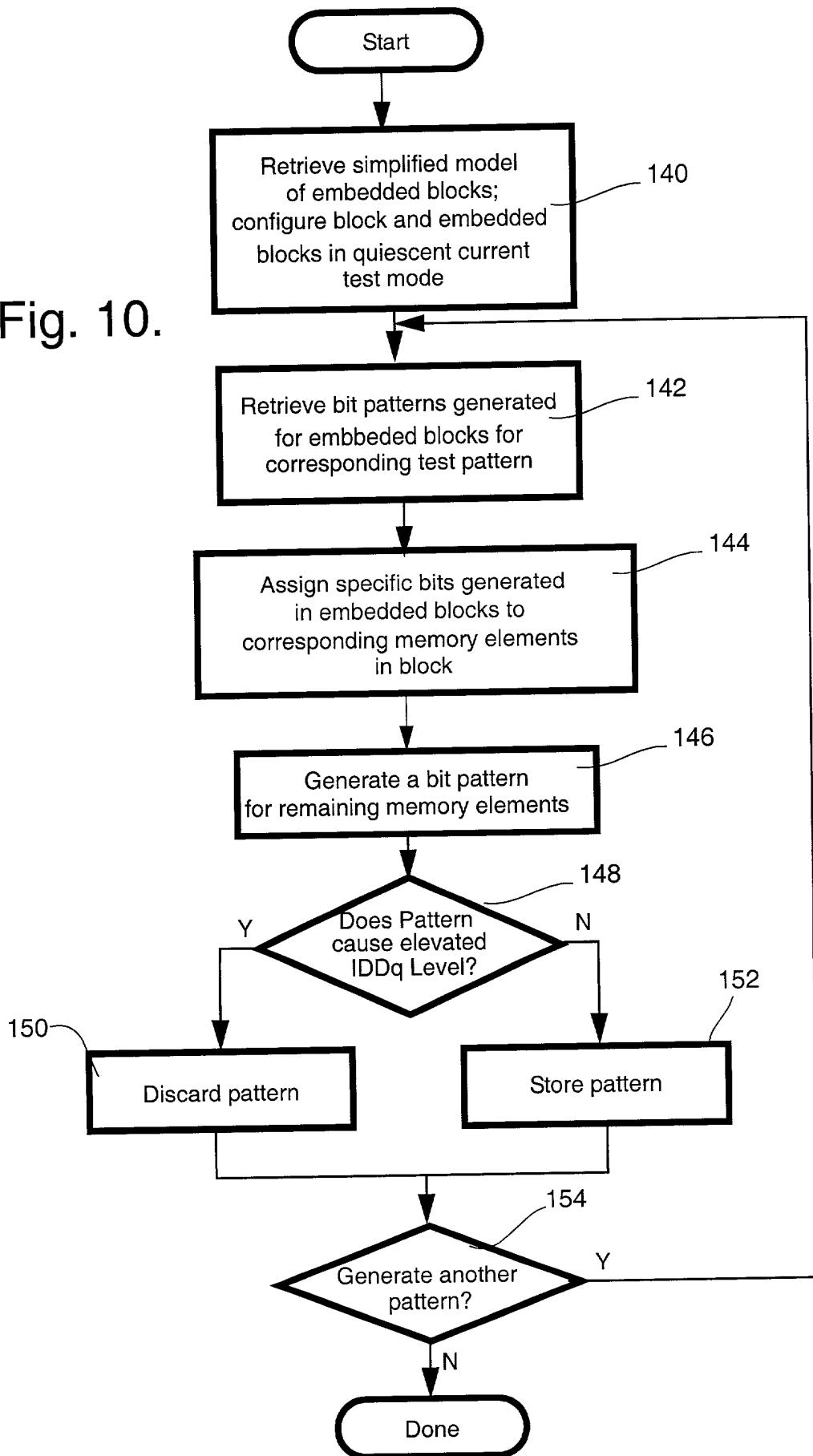


Fig. 10.



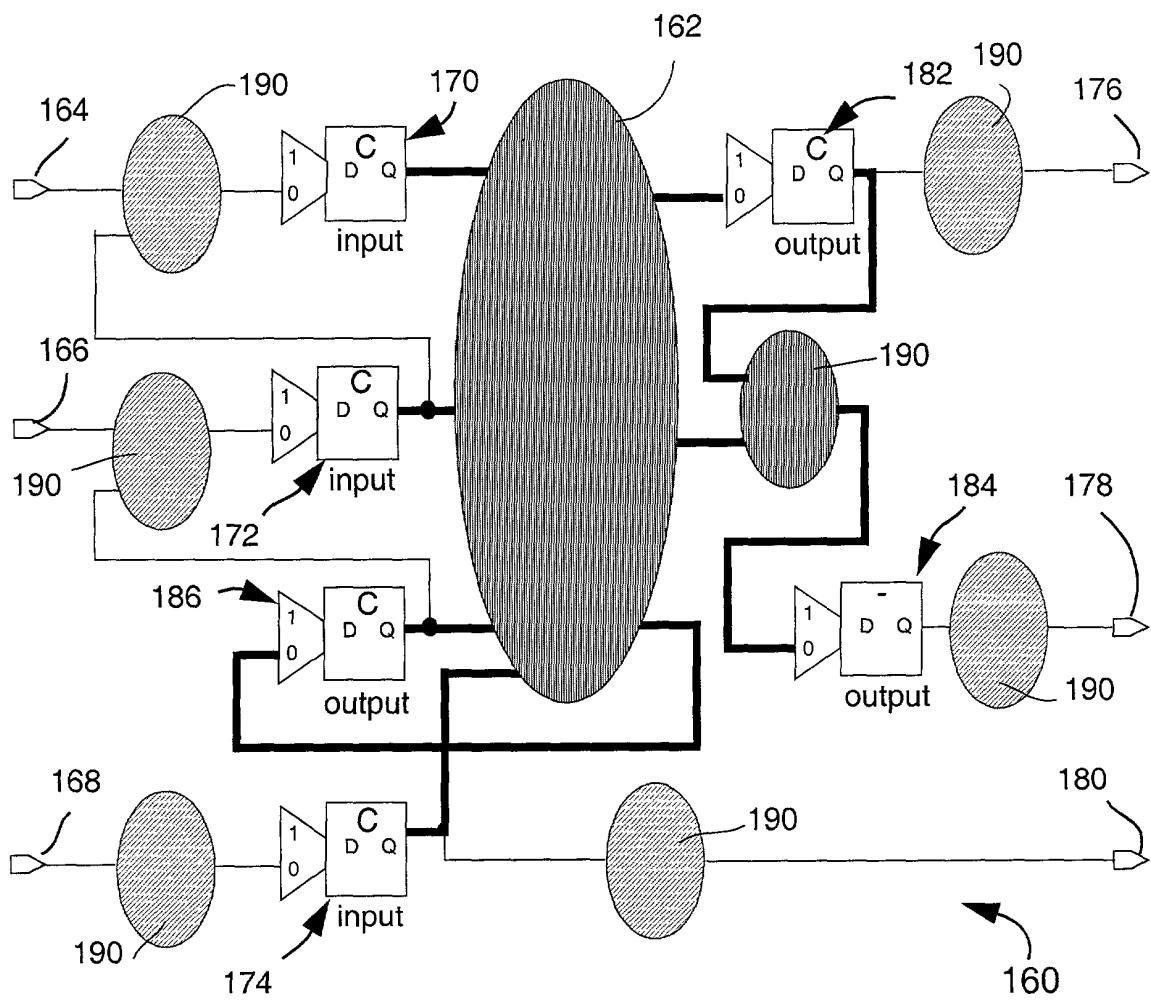


Fig. 11.

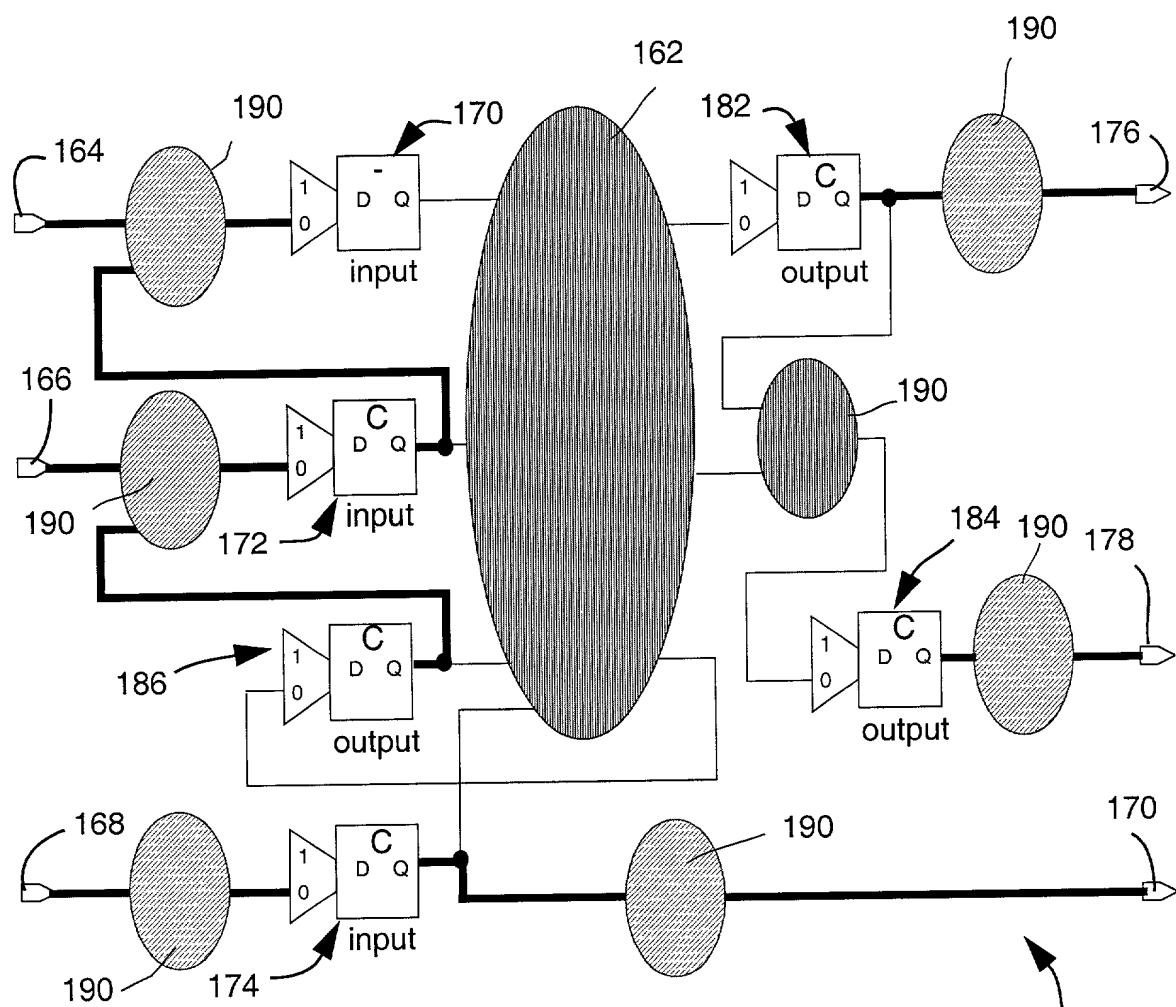


Fig. 12.

■ internal logic
 ▨ peripheral logic

Fig. 13.

TABLE 1. IDDq patterns for configuration of figure 11

Fxxx	Fxxy	F170	F172	F174	F182	F184	F186	Fxxz	Fxxt
0	1	1	X	0	0	X	1	0	1
1	1	0	1	X	1	X	0	0	0
0	X	X	0	1	X	1	X	1	0
X	0	0	0	1	1	0	0	X	1
1	0	1	X	X	X	X	X	0	X
1	0	1	X	X	X	X	X	0	X

TABLE 2. IDDq patterns for configuration of figure 12

Fyyy	Fyyx	Fyyz	F172	F174	F182	F184	F186	Fyyt	Fyyu	Fzzx	Fzy
1	1	0	1	0	0	0	1	0	1	1	0
1	1	0	1	0	1	1	0	0	0	0	1
0	X	X	0	1	0	1	1	1	0	X	1
X	0	0	0	1	1	0	0	X	1	0	X
0	1	0	1	0	0	0	1	0	0	1	1
1	0	X	0	0	1	1	1	X	1	0	0

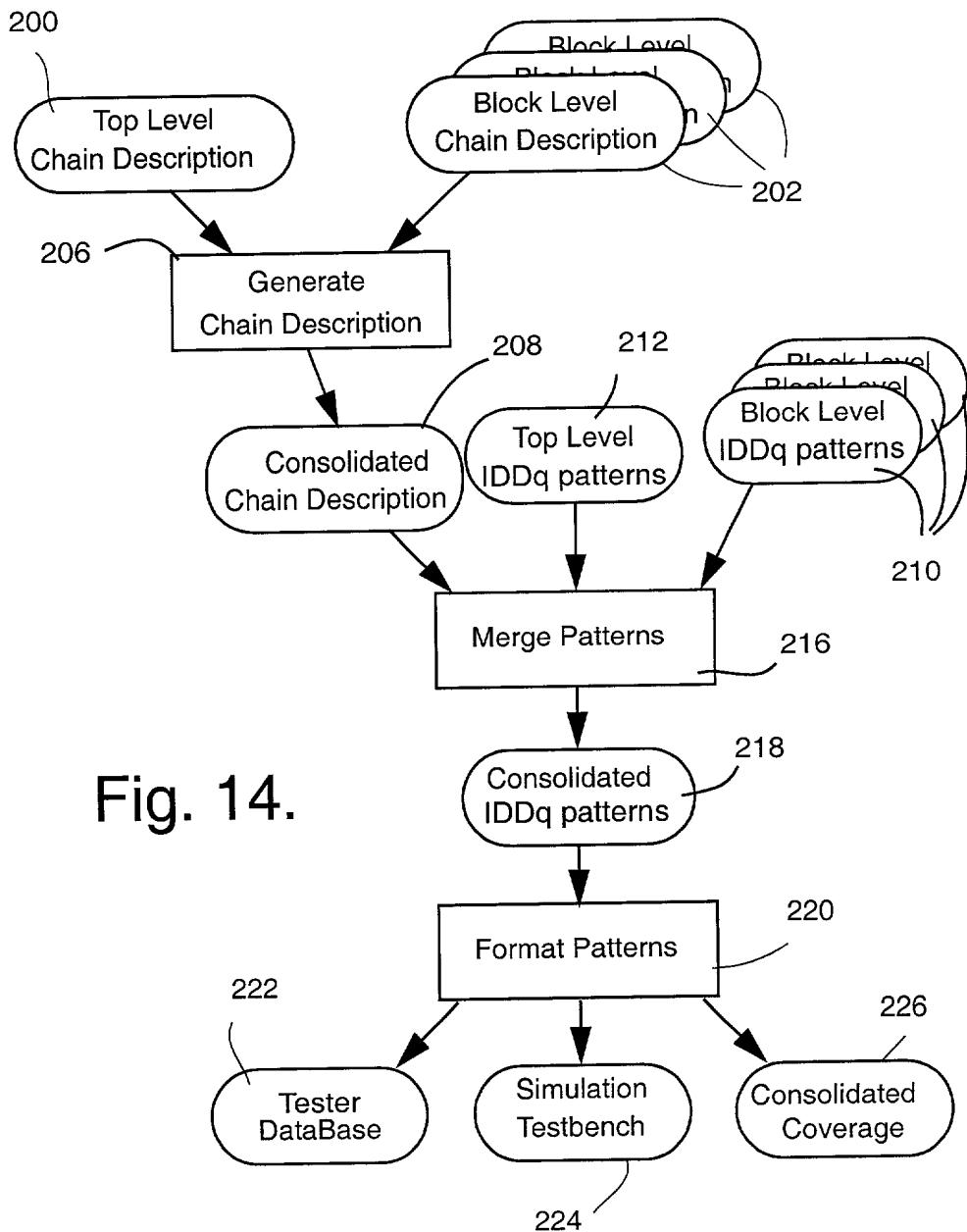
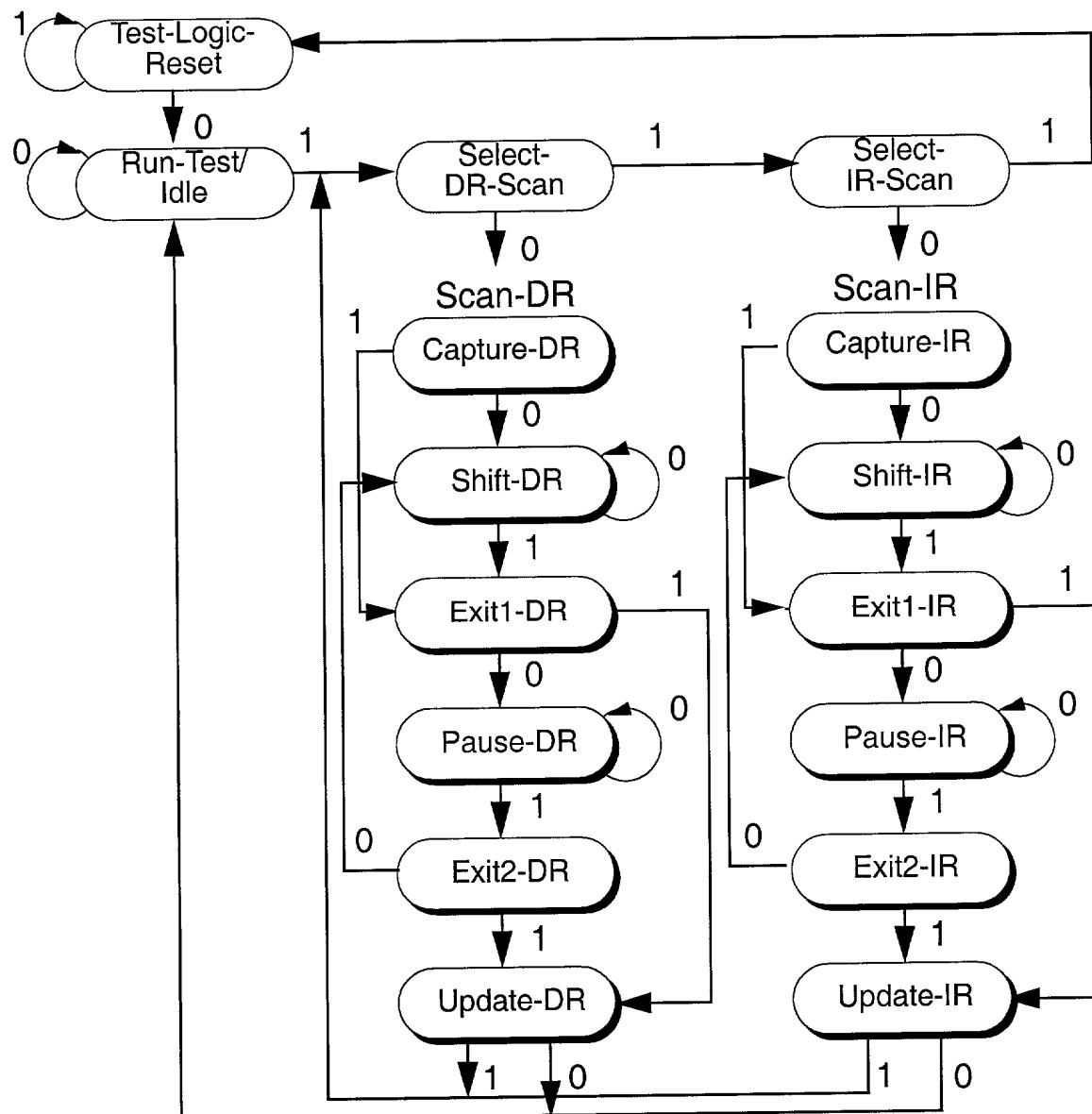


Fig. 14.



NOTE: The values adjacent to each state transition correspond to *TMS*.

Fig. 15.
(Prior Art)